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Research Article

New Pulse Width Modulation Technique to Reduce Losses for Three-Phase Photovoltaic Inverters

Mohannad Jabbar Mnati,[1,2] **Dimitar V. Bozalakov**,[1] **and Alex Van den Bossche**[1]

[1]*Department of Electrical Energy, Metals, Mechanical Constructions and Systems, Ghent University, Technologiepark Zwijnaarde 913, B-9052 Zwijnaarde, Gent, Belgium*
[2]*Department of Electronic Technology, Institute of Technology Baghdad, Middle Technical University, Al-Za'franiya, 10074 Baghdad, Iraq*

Correspondence should be addressed to Mohannad Jabbar Mnati; mohannad.mnati@ugent.be

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Nowadays, most three-phase, "off the shelf" inverters use electrolytic capacitors at the DC bus to provide short term energy storage. However, this has a direct impact on inverter lifetime and the total cost of the photovoltaic system. This article proposes a novel control strategy called a 120° bus clamped PWM (120BCM). The 120BCM modulates the DC bus and uses a smaller DC bus capacitor value, which is typical for film capacitors. Hence, the inverter lifetime can be increased up to the operational lifetime of the photovoltaic panels. Thus, the total cost of ownership of the PV system will decrease significantly. Furthermore, the proposed 120BCM control strategy modulates only one phase current at a time by using only one leg to perform the modulation. As a result, switching losses are significantly reduced. The full system setup is designed and presented in this paper with some practical results.

1. Introduction

Constantly growing concerns about global warming have forced many countries to change their energy policy towards increasing the share of renewable energy resources and hence reducing CO2 emissions. Significant amounts of these renewable energy resources are delivered by photovoltaic (PV) systems with small and medium power, interfaced with the distribution grid via power electronic voltage source inverters. In order to bring maximum revenue to the prosumer during the lifetime of the PV system, the power electronic inverter must have as high efficiency as possible and as long a life as possible, at a limited cost. A typical photovoltaic panel has a useful lifetime of 25 years. The inverter lifespan of roughly 10 years is limited, however, primarily due to electrolytic capacitor lifetime. Hence, typically, three inverters will be needed during the exploitation period of a PV system. [1, 2].

The efficiency of a typical power electronic inverter that uses hard switching commutation varies between 95% and 98%, depending on the power electronic switches used (MOSFET, IGBT, SiC, etc.) and power ratings. To increase efficiency, losses in the semiconductor switches and the magnetic components (the output inductive filter) must be reduced. Semiconductor losses can be split into conduction and switching losses. Conduction loss can be reduced by selecting switches with a lower voltage drop across them; nevertheless it is always present. Switching losses, however, can be reduced or even eliminated by using soft-switching techniques such as zero-voltage and zero-current commutation; in [3], the authors achieved peak efficiency of 97% and in [4], 98.4%. Soft switching operates with limited dv/dt and/or di/dt, which have an advantageous effect on electromagnetic compatibility issues, reduces the thermal stresses on the power electronic switches, and combined with the limited dv/dt and/or di/di have a positive impact on the inverter lifetime. Some of the main drawbacks of these techniques are (i) operating at rather fixed loads [3, 5], which is not the case in photovoltaic systems, due to the intermittent nature of solar irradiation; (ii) requiring additional components and control signals [3, 6], which increases the control complexity and physical implementation of the power electronic inverter; and (iii) operating under a variable carrier frequency [6–8], which introduces filtration problems. In [8], a power

electronic inverter topology is proposed using hard switching techniques, based on MOSFET and IGBT combination per leg.

The approach uses the MOSFET to perform the current modulation and it is switched with the nominal carrier frequency, while the IGBT is switched with the grid frequency. The advantage of the better free-wheeling IGBT diode is used in this approach, and the authors report decreasing the switching losses by 33%. The advantage of this approach is that no additional components or complex controls are required, which renders the approach extremely attractive. Another possibility for reducing switching losses is to use space vector modulation with 60° bus clamping, as studied in [1, 9]. This is effective at high AC voltage output, where it reduces total switching cycles by one-third. Although the above-mentioned techniques offer increased efficiency, if used in PV applications, they still require a significant amount of filtering capacitance at the DC bus, which limits the lifetime of the power electronic inverter.

An alternative to electrolytic capacitors is film capacitors, which have a lifetime comparable to PV panels, but is not an economically viable solution, due to their small capacitance to price and capacitance to volume ratios. In [9], a control algorithm is proposed that uses two film capacitors of 33 μF connected in a symmetrical half bridge power electronic converter, with dual voltage compensation for stabilizing the DC bus voltage. The proposed approach is tested on a 1 kW inverter, and the results show that the 100 Hz ripple at the DC bus can be completely compensated for in steady state operation, with a minimum capacitance of 33 μF required. The additional control plus the converter react in such a way that capacitance is increased; i.e., the converter includes additional virtual capacitance in the system. Hence, this solution appears particularly suitable for replacing the electrolytic capacitors at the DC side. A disadvantage of the approach is that stabilization is performed via additional hardware, which requires additional space in physical implementation, as well as extra control signals.

In [1], a novel control strategy for a single-phase PV inverter is proposed, which is implemented on a three-phase IGBT module. The inverter consists of an input boost converter (one leg of the module), a film capacitor at the DC bus, and full bridge inverter (leg two and three of the module), the outputs of which are connected to the grid through an LC filter. The control strategy injects the phase current in two stages; i.e., when the grid voltage is lower than the PV voltage, the control strategy drives only the full bridge to modulate the phase current. When the grid voltage is higher than the PV voltage, the control strategy starts controlling the boost converter. By doing so, the boost converter ensures a DC bus voltage margin to the full bridge inverter, which is sufficient for guaranteeing normal current injection into the grid. This control strategy is able to reduce bridge switching losses approximately six times, compared to a state of nonbus clamped control. The other advantage is that the control strategy is implemented on an inverter that uses a film capacitor, which ensures a lifetime comparable with the lifetime of the PV. Moreover, the film capacitor that is used has a value of 22 μF, which is smaller compared to that used in [9] and is suggested as a possible minimum value.

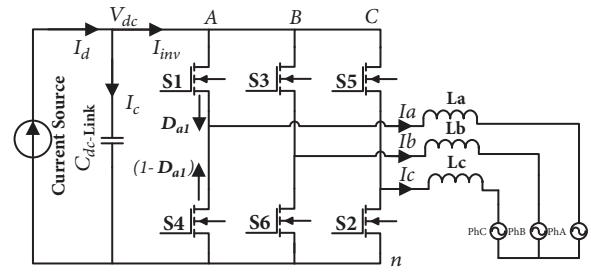


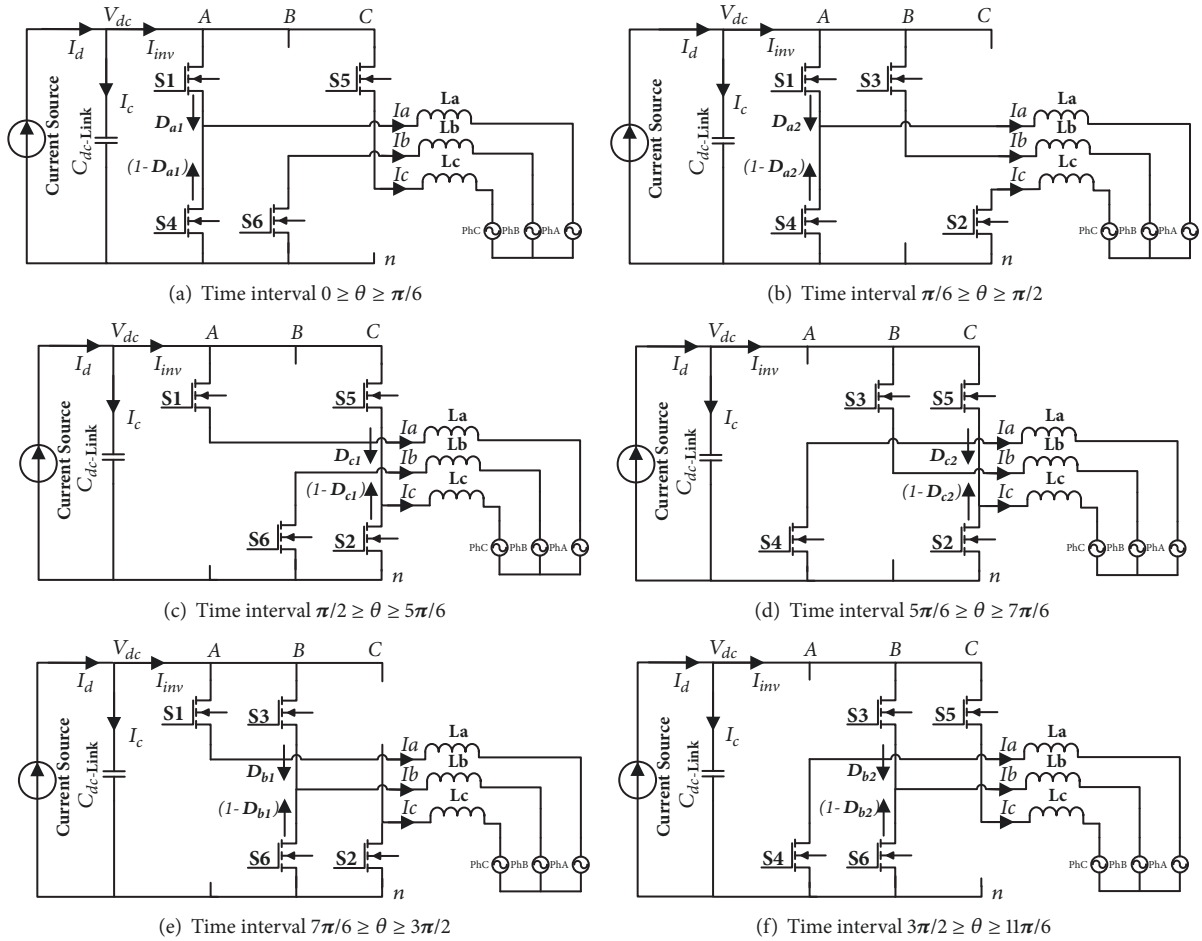
Figure 1: Three-phase inverter 120BCM with modulated DC link.

In this paper, a control strategy for a three-phase inverter is proposed that uses a similar approach as [1]. The control is verified by means of simulations in MATLAB/Simulink and practical full system setup on a three-phase, three-leg inverter. The experiments were performed using the experimental setup to verify the performance of the proposed control strategy (a 120° bus clamped PWM (120BCM)). The experimental setup consists of three-phase inverter with L filter and a control board, power board, and voltage and current sensors for DC and AC sides [10, 11]. The control board is composed of dsPIC microcontroller dsPIC33FJ256GP710A and it is the main unit used in the implementation to control the three-phase inverter. It is programmed by MPLAB X IDEV3.15 software compiler and C language.

This paper is organized as follows. Section 2 provides a detailed description of the proposed control strategy and the different time intervals are described. Section 3 provides a detailed simulation of the presented control algorithm, and different modulation strategies are compared using numerical calculations of the switching losses. Section 4 presents the simulation result with details. Section 5 presents the practical of three-phase inverter with results and finally Section 6 presents conclusions of the article.

2. 120° Bus Clamped PWM System Configuration

Natural sampling and centered PWM modulations commutate the semiconductor switches during the entire period of the fundamental current. Thus, if no special measures are taken such as ZVS and ZCS, switching losses are often larger than conduction losses. The proposed PWM technique (120BCM) is based on a partial modulation of the injected phase current; thereby, switching losses can be significantly reduced, compared to the classical PWM technique. In order to evaluate the performance of the 120BCM, the topology presented in Figure 1 is used. This is a classical three-phase inverter topology and is connected to the grid through a star connection. The DC bus capacitor is low value film-based, which, as noted above, will have a beneficial effect on inverter lifetime. Three inductors are used to filter out the current pulsation caused by the modulation frequency. Prior to starting the operational principle, the following assumptions are considered in this paper:



(a) Time interval $0 \geq \theta \geq \pi/6$

(b) Time interval $\pi/6 \geq \theta \geq \pi/2$

(c) Time interval $\pi/2 \geq \theta \geq 5\pi/6$

(d) Time interval $5\pi/6 \geq \theta \geq 7\pi/6$

(e) Time interval $7\pi/6 \geq \theta \geq 3\pi/2$

(f) Time interval $3\pi/2 \geq \theta \geq 11\pi/6$

Figure 2: Six switching configurations in 120° BC-PWM control method.

(1) The inverter is supplied with a current source. In practice, this assumption holds if there is a matching circuit (for example, a boost converter) between the renewable source and the inverter that will guarantee maximum power point operation, as well as a current source output characteristic.

(2) It is assumed that the input instantaneous power is constant.

(3) For the sake of maintaining clarity, the matching block between the renewable energy source and the inverter is not considered in this paper.

(4) Only positive-sequence current injection is considered; hence, the instantaneous value of the sum of the three currents is zero.

(5) The inverter operates in a steady state mode.

As noted above, the operational principle of the 120BCM is based on partial modulation of the injected phase current. When only positive-sequence current is being injected, a natural zero crossing of the phase currents occurs every 60 electrical degrees. Considering the above assumptions, the 120BCM operational principle can be explained as follows.

(i) Interval $0^\circ \leq \theta \leq 30^\circ$. This interval begins when the zero crossing of phase current i_a occurs (i_a becomes positive) and the duration of it is 30°. The state of the switches during the first interval is depicted in Figure 2(a), where it can be seen that switches S1, S4, S5, and S6 are being controlled. The modulation for the injected phase currents i_a, i_b, and i_c is performed only by switches S1 and S4, while the other two switches are kept continuously closed. Considering this and the above listed assumptions, the injected currents in this interval can be expressed in

$$D_{a1} = \frac{v_a - v_b}{V_{dc}} = \frac{v_a - v_b}{v_c - v_b} \tag{1}$$

$$\begin{aligned} i_{b1} &= i_{inv} + D_{a1} i_{a1} \\ i_{c1} &= i_{inv} + \left(1 - D_{a1}\right) i_{a1} \end{aligned} \tag{2}$$

where D_{a1} is a duty ratio and i_b and i_c are the modulated phase currents in this interval and i_{inv} is the input inverter current. Since S5 and S6 are closed continuously, the DC bus capacitor is connected to the line-to-line voltage Vbc. However, the line current that flows through it is almost negligible compared to the phase currents, as the DC bus capacitors are rather small (this study uses a DC bus capacitor of 8 μF). Following this

Table 1: Mathematical description of the proposed BCPWM technique during the different intervals.

Interval	Equation	Interval	Equation
$(V_{PhB} \geq V_{PhA} \geq V_{PhC})$ $0 \geq \theta \geq 30^{\circ}$ $330^{\circ} \geq \theta \geq 360^{\circ}$ Figure 2(a)	$D_{a1} = \frac{V_a - V_b}{V_{dc}} = \frac{V_a - V_b}{V_c - V_b}$ $i_{b1} = i_{inv} + D_{a1} i_{a1}$ $i_{c1} = i_{inv} + (1 - D_{a1}) i_{a1}$	$(V_{PhC} \geq V_{PhA} \geq V_{PhB})$ $150^{\circ} \geq \theta \geq 210^{\circ}$ Figure 2(d)	$D_{a2} = \frac{V_a - V_c}{V_{dc}} = \frac{V_a - V_c}{V_b - V_c}$ $i_{b2} = i_{inv} + (1 - D_{a2}) i_{a2}$ $i_{c2} = i_{inv} + D_{a2} i_{a2}$
$(V_{PhB} \geq V_{PhC} \geq V_{PhA})$ $30^{\circ} \geq \theta \geq 90^{\circ}$ Figure 2(b)	$D_{c1} = \frac{V_c - V_b}{V_{dc}} = \frac{V_c - V_b}{V_a - V_b}$ $i_{a1} = i_{inv} + (1 - D_{c1}) i_{c1}$ $i_{b1} = i_{inv} + D_{c1} i_{c1}$	$(V_{PhA} \geq V_{PhC} \geq V_{PhB})$ $210^{\circ} \geq \theta \geq 270^{\circ}$ Figure 2(e)	$D_{c2} = \frac{V_c - V_a}{V_{dc}} = \frac{V_c - V_a}{V_b - V_a}$ $i_{a2} = i_{inv} + D_{c2} i_{c2}$ $i_{b2} = i_{inv} + (1 - D_{c2}) i_{c2}$
$(V_{PhC} \geq V_{PhB} \geq V_{PhA})$ $90^{\circ} \geq \theta \geq 150^{\circ}$ Figure 2(c)	$D_{b1} = \frac{V_b - V_c}{V_{dc}} = \frac{V_b - V_c}{V_a - V_c}$ $i_{a1} = i_{inv} + (1 - D_{b1}) i_{b1}$ $i_{c1} = i_{inv} + D_{b1} i_{b1}$	$(V_{PhA} \geq V_{PhB} \geq V_{PhC})$ $270^{\circ} \geq \theta \geq 330^{\circ}$ Figure 2(f)	$D_{b2} = \frac{V_b - V_a}{V_{dc}} = \frac{V_b - V_a}{V_c - V_a}$ $i_{a2} = i_{inv} + D_{b2} i_{b2}$ $i_{c2} = i_{inv} + (1 - D_{b2}) i_{b2}$

Table 2: Switching states of the proposed 120 BCM.

One Cycle (360°)	Leg A S1 and S4	Leg B S3 and S6	Leg C S5 and S2
$0^{\circ} \leq \theta \leq 30^{\circ}$ $330^{\circ} \leq \theta \leq 360^{\circ}$	PWM	0-1	1-0
$30^{\circ} \leq \theta \leq 90^{\circ}$	1-0	0-1	PWM
$90^{\circ} \leq \theta \leq 150^{\circ}$	1-0	PWM	0-1
$150^{\circ} \leq \theta \leq 210^{\circ}$	PWM	1-0	0-1
$210^{\circ} \leq \theta \leq 270^{\circ}$	0-1	1-0	PWM
$270^{\circ} \leq \theta \leq 330^{\circ}$	0-1	PWM	1-0

period of 30°, switch S1 is closed (clamps the DC bus) for 120° and modulation is performed by another leg. For this reason, the proposed PWM control strategy is referred to as 120° bus clamped modulation.

(ii) Interval $30^{\circ} \leq \theta \leq 90^{\circ}$. This interval begins 30° after the zero crossing of phase current i_a occurs (i_a becomes positive) and its duration is 60°. The states of the switches during the first interval are depicted in Figure 2(c), where it can be seen that switches S1, S6, S5, and S2 are being controlled. The modulation for the injected phase currents i_a, i_b, and i_c is again performed only by switches S5 and S2, while switches S1 and S6 are kept continuously closed. The injected currents in this interval can be expressed in

$$D_{c1} = \frac{V_c - V_b}{V_{dc}} = \frac{V_c - V_b}{V_a - V_b} \tag{3}$$

$$\begin{aligned} i_{a1} &= i_{inv} + \left(1 - D_{c1}\right) i_{c1} \\ i_{b1} &= i_{inv} + D_{c1} i_{c1} \end{aligned} \tag{4}$$

The operational principle concerning the remaining 4 intervals $90^{\circ} \leq \theta \leq 150^{\circ}$, $150^{\circ} \leq \theta \leq 210^{\circ}$, $210^{\circ} \leq \theta \leq 270^{\circ}$, and $270^{\circ} \leq \theta \leq 330^{\circ}$ is similar to the described above. The corresponding equivalent circuits are Figures 2(b), 2(d), 2(e), and 2(f). For more clarity all mathematical equations describing the different intervals are listed in Table 1 and a summary of all switching states is given in Table 2. As can be seen form Figure 2 and Table 2 during all 6 intervals (60° each), the phase currents are always modulated only by one leg of the power electronic inverter. Thus the total commutations for the entire inverter are decreased 3 times compared to the classical full sine PWM technique. Hence, in general the total switching losses will also decrease. It occurs at a typical current of 0 to 50% of the peak current value. In the simplified assumption that the switching losses would be proportional to voltage and current, the ratio is approximated.

Integral sine −30° to +30° /integral sine −90° to 90° is

$$\begin{aligned} &\frac{(1 - \cos(\pi/6))}{(\cos(0) - \cos(\pi/2))} \\ &\quad = 13.4\% \text{ compared to centred PWM} \\ &\frac{(1 - \cos(\pi/6))}{(\cos(0) - \cos(\pi/23))} \\ &\quad = 26.8\% \text{ compared to } 60^{\circ} \text{ bus clamped PWM} \end{aligned} \tag{5}$$

The reality is that switching losses are less than proportional to current, but that the DC link voltage is also typically 15% reduced, so that at least a factor 3-4 reduction occurs in switching loss compared to a 60° bus clamped PWM and 4-8 compared to a centered PWM. The exact value depends on the detailed transistor data and on the way it is controlled.

Note that the duration of the first interval is also 60° and the full length of this interval is $330^{\circ} \leq \theta \leq 30^{\circ}$ but for simplicity 0° was chosen for a starting point.

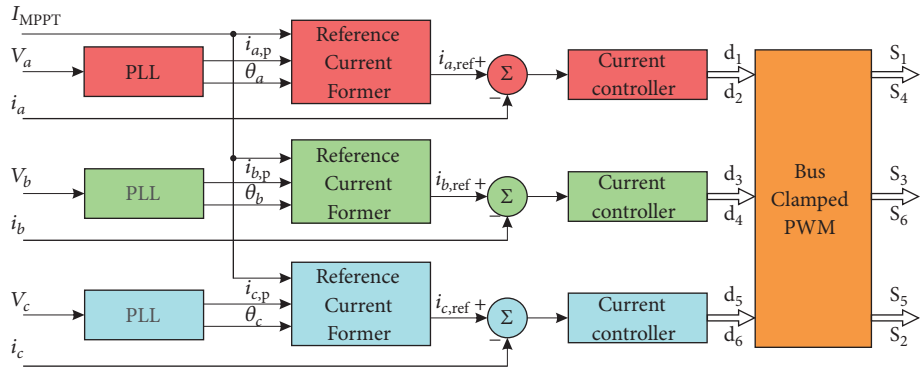


Figure 3: Block diagram of the control block of the BCPWM technique.

3. Control Principle of the BCPWM

The designed controller for the power electronic switches equipped with the BCPWM is depicted in Figure 3. The phase angles are extracted from the three-phase voltages using a three-phase locked loop (PLL). The output off the PLL generates three synchronized voltages with the phase voltages and reference amplitude of 1V. The reference current of each phase is created using the PLL signal for the corresponding phase, which is multiplied with the maximum allowed current that can be delivered by the primary source (PV) determined by the MPPT (the MPPT is outside the scope of this work). Then, the reference current is subtracted from the measured phase current, giving an error current signal. This error is passed to a conventional proportional-integral (PI) controller. The output signal of the PI controller is compared with a triangular signal and the modulated signal is processed by a block, where the 120BCM modulation is embedded. In this block, Boolean logic is used to implement the 60° modulations, where the logic equations are derived as shown in (6) to (11).

The "+" means logical OR, multiplication means logical AND, the operators "<" and ">" are used to represent the conditional function "if", $i_{x,p}$ is the instantaneous value of respective reference currents delivered by the PLL, and PWM is the signal generated by the comparison between the PI output and the triangular signal, as shown in Figure 5. In this study, dead time is neglected; however, in real implementation, this should be taken into account.

$$\begin{aligned} S_{1,PWM} &= \left(i_{a,p} > i_{b,p}\right)\left(i_{a,p} > i_{c,p}\right) \\ &\cdot \left(\left(i_{b,p} \geq i_{a,p}\right)\left(i_{a,p} \geq 0\right) + \left(i_{c,p} \geq i_{a,p}\right)\left(i_{a,p} \leq 0\right)\right. \\ &\left. + \left(i_{c,p} \geq i_{a,p}\right)\left(i_{a,p} \geq 0\right) + \left(i_{b,p} \geq i_{a,p}\right)\left(i_{a,p} \leq 0\right)\right) \\ &\cdot PWM \end{aligned} \tag{6}$$

$$S_{4,PWM} = \overline{S_{1,PWM}} \tag{7}$$

$$\begin{aligned} S_{2,PWM} &= \left(i_{b,p} > i_{a,p}\right)\left(i_{b,p} > i_{c,p}\right) \\ &\cdot \left(\left(i_{c,p} \geq i_{b,p}\right)\left(i_{b,p} \geq 0\right) + \left(i_{a,p} \geq i_{b,p}\right)\left(i_{a,p} \leq 0\right)\right. \\ &\left. + \left(i_{a,p} \geq i_{b,p}\right)\left(i_{b,p} \geq 0\right) + \left(i_{b,p} \geq i_{c,p}\right)\left(i_{c,p} \leq 0\right)\right) \\ &\cdot PWM \end{aligned} \tag{8}$$

$$S_{5,PWM} = \overline{S_{2,PWM}} \tag{9}$$

$$\begin{aligned} S_{3,PWM} &= \left(i_{c,p} > i_{b,p}\right)\left(i_{c,p} > i_{a,p}\right) \\ &\cdot \left(\left(i_{a,p} \geq i_{c,p}\right)\left(i_{c,p} \geq 0\right) + \left(i_{c,p} \geq i_{b,p}\right)\left(i_{c,p} \leq 0\right)\right. \\ &\left. + \left(i_{b,p} \geq i_{c,p}\right)\left(i_{c,p} \geq 0\right) + \left(i_{c,p} \geq i_{a,p}\right)\left(i_{a,p} \leq 0\right)\right) \\ &\cdot PWM \end{aligned} \tag{10}$$

$$S_{6,PWM} = \overline{S_{3,PWM}} \tag{11}$$

4. Validation of the Proposed 120BCM Technique by Means of Simulation

The performance of the 120BCM is evaluated in a simulation environment using MATLAB-Simulink. The connection diagram for the three-phase inverter equipped with the 120BCM control algorithm is depicted in Figure 1. The three-phase inverter is supplied with a DC current of 13.5A and it is connected to the grid via three differential inductor filters, L_a, L_b, and L_c. The grid is represented by a line impedance of 0.1+j0.0314, which is a typical impedance value for low voltage distribution grids [12, 13] and an ideal three-phase voltage source. Detailed data concerning the connection diagram is shown in Table 3.

4.1. Simulation Results. The driving pulses used by S1 and S4 generated by the PWM block are depicted in Figure 4, where it can be seen that the driving pulses are present during the first 1/6th and 5/6th of the period. This interval is described in Figures 2(a) and 2(b). The current that flows through switches S1 and S4 is also depicted in Figure 6.

As can be seen, the modulation of the current injected in phase (a) is being modulated only in the first and last 30° interval of the half-wave, while the rest of the current waveform is being modulated by the remaining legs of the inverter. In the transition intervals, a small transient of

Table 3: Data used in the Simulink model.

Parameter	Value
Grid Voltage	400V(L-L)
Grid Frequency f_g	50Hz
Line impedance	0.1+j0.0314
Filter Inductor L_a, L_b, L_c	2.5mH
Switching Frequency	25kHz
Film capacitor C_{dc}	8 μF
Inverter rms dc current I_{inv}	13.5A
Total injected active power	6.6 kW

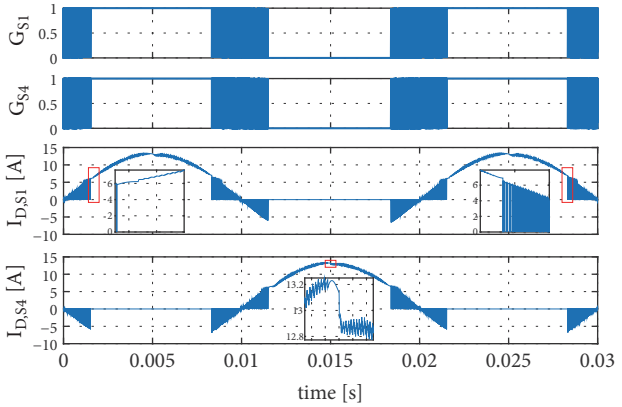


Figure 4: The modulation of the current injected in phase (A).

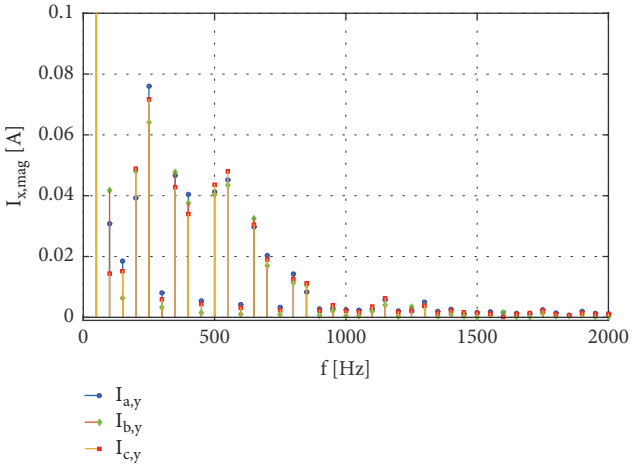


Figure 5: Harmonic content of the three-phase currents where y $\in$ [1..40]-IEC61000-3-2.

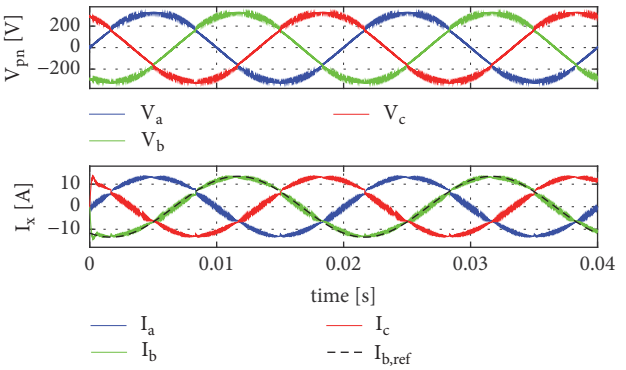


Figure 6: Phase voltages at the inverter terminals, injected phase currents, and reference current comparison.

the current occurs, which is also shown in Figure 4. These transients are always present when the 120BCM switches between time intervals, which is the reason for the small transient at the top of the sine wave of the injected current. The other phase currents, i_b and i_c, have identical waveforms, but are 120° phase shifted.

Another important aspect of the grid connected inverters is their total harmonic distortion limit (THD). According to IEC 61000-3-2 [14], the THD of the inductor currents must not exceed 5%. Due the small transients between the different intervals, a spectrum analysis is performed on the phase currents, which is depicted in Figure 5. The harmonics under investigation range from fundamental up to the 41st harmonic, which is the maximum covered by [14].

The fundamental peaks up to 13.6 A, which is its nominal value; however, more attention is paid to higher order harmonics. Figure 5 shows that the higher order harmonics magnitude is relatively low, complying with [14]. Furthermore, despite the partial modulation technique (60 electrical degrees per interval), the THD for each phase does not exceed 2.9%, which complies with [14] and makes the proposed 120BCM extremely suitable for renewable energy applications.

Finally, the obtained simulation results of the phase voltages at the inverter terminals and the injected currents are presented in Figure 6. The results show that despite the current being modulated in split intervals using independent controllers, the wave forms have pure sinusoidal forms with very small distortions. Furthermore, the reference current $I_{b,ref}$ is depicted on the top of the injected ones by the black dashed line, and it is noted that the PI controller is able to track the reference currents very well, without the need for feed forward controls, which significantly simplifies practical implementation. The other two reference currents are also tracked with the same performance, but are not depicted in Figure 6.

As noted above, the three-phase inverter connection is without a neutral. The simulation results obtained for the DC bus voltage are shown in Figure 7, together with the line-to-line voltages V_{ab}, V_{bc}, and V_{ca}, as well as the inverter voltage, which in this particular modulation technique is a sufficient margin to allow for proper current injection into input current I_{inv}. It is noted that the DC bus voltage has three-phase full bridge rectifier; additionally, it can be seen that the DC bus voltage is slightly higher that the line-to-line waveform, significantly resembling the one obtained after a grid. A standard inverter will need a margin of 10V to 20V between the peak value of the grid line-to-line voltage and the DC bus voltage [13]. Additionally, taking into account the grid voltage fluctuation set by EN50160 [15], which allows for a 10% upper threshold, the DC bus voltage becomes at least

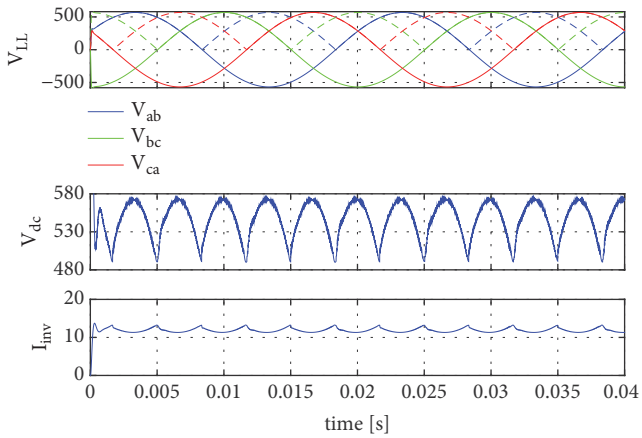


FIGURE 7: Obtained simulation results of the dc bus voltage V_{dc} and inverter dc bus current I_{inv}.

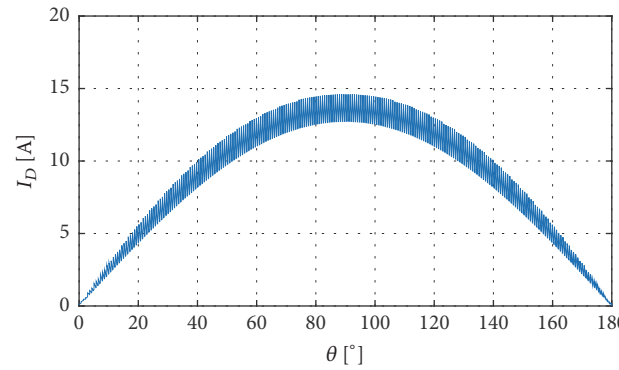


FIGURE 8: Current ripple during one half-sine, used for the loss switching calculation.

620V, and the margin mentioned above the final value will be at least 630 V.

4.2. Switching Loss Calculation in Semiconductor Devices. Switching loss calculation can sometimes be a difficult endeavor, especially when PWM is involved. Since the majority of losses of the inverter are composed of conduction losses, switching losses, and losses in the magnetic material in the magnetic components (output filters), then it is very difficult to segregate and evaluate each loss independently by means of experiment. Furthermore, the assessment of each of the losses becomes even more difficult because of the different modulation intervals that are introduced by the partial modulation of 120BCM and 60PWM. Therefore, a numerical calculation can be used to assess the switching losses so that an easy and fast evaluation can be performed. In [12], the author proposes a cycle-by-cycle calculation for switching losses, and then the individual losses are summarized. This method provides quite accurate results; however, it is designed for central modulation. In [16], a methodology of loss calculation is presented that uses linear approximations to obtain the different parameters, such as turn-on and turn-off energy, needed for the switching loss calculation, with satisfying results. In this article a combination of the cycle-by-cycle approach and linear approximation of the required parameters are used to calculate the losses of the different PWM techniques. Based on these two approaches, the following equation for losses calculation of the half-sine modulated signal for 0° to 180° is obtained:

$$P_{tot} = \left(\sum_{0}^{n} E_{on} \left(\frac{i_{on}(n)}{I_D} \right)^{\alpha} \left(\frac{V_{dc}(n)}{V_{cc}} \right)^{\beta} + \sum_{0}^{n} E_{off} \left(\frac{i_{on}(n)}{I_D} \right)^{\alpha} \left(\frac{V_{dc}(n)}{V_{cc}} \right)^{\beta} \right) 2 f_g \tag{12}$$

where E_{on} is the turn-on energy loss, E_{off} is the turn-off energy loss, $i_{on}(n)$ is the instant value of the current at turn-on, $i_{off}(n)$ is the instant value of the current at turn-off, I_D is the drain current and V_{CC} is the voltage at which the energy is measured, and $V_{dc}(n)$ is the instant value of the DC bus voltage. Since this is the loss calculated for one half period, a transistor, multiplication by two is needed to obtain the full leg period. Suppose that the current flowing through the switches is the one shown in Figure 8 where the current ripple plus the fundamental are used in (12), and also the switching loss has been taken proportional to current (corresponding with the data) and linear approximations are used to calculate the losses as suggested in [17]. The exponent coefficients α and β represent the current and voltage dependency of the variation from the nominal values used in the datasheets. A special case is formed: if α=1 and β=1, then the switching losses are linear with the variation from the nominal values. According to [18] for IGBT switches the current dependency is α=1 which is a linear approximation while β=1.2..1.4. Nevertheless, these coefficients are dependent on the transistor manufacturer and also transistor type. In [19–22], more accurate methodologies for assessing the switching losses are proposed; however, their drawback is the high complexity and also difficulty to being implemented in practice.

It was noted previously that a standard inverter needs some degree of a DC bus voltage margin. However, to better assess the performance of the different modulation control strategies, the DC bus voltage for all three calculations is kept at 560V. The switching losses equation used for the 60° bus clamped method is similar to (12), but the switches clamp to the DC bus voltage for a 60° period, where switching losses are not present. Then (12) can be rewritten as

$$P_{tot} = \left(\sum_{0}^{\pi/3} E_{on} \frac{i_{on}(n)}{I_D} \frac{V_{dc}(n)}{V_{cc}} + \sum_{2\pi/3}^{n} E_{on} \frac{i_{on}(n)}{I_D} \frac{V_{dc}(n)}{V_{cc}} + \sum_{0}^{\pi/3} E_{off} \frac{i_{off}(n)}{I_D} \frac{V_{dc}(n)}{V_{cc}} + \sum_{2\pi/3}^{n} E_{off} \frac{i_{off}(n)}{I_D} \frac{V_{dc}(n)}{V_{cc}} \right) 2 f_g \tag{13}$$

The switching losses for 120BCM can be calculated by (13), but the intervals must be changed $\pi/6$ for the first part of the half-sine and $5\pi/6$ for the last part of the half-sine. In this

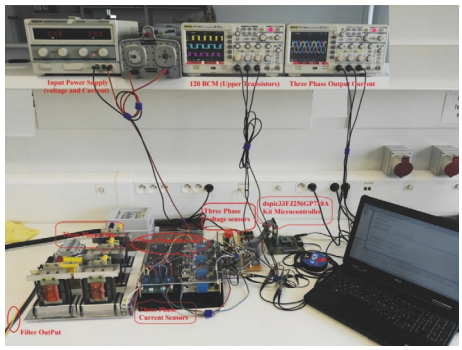
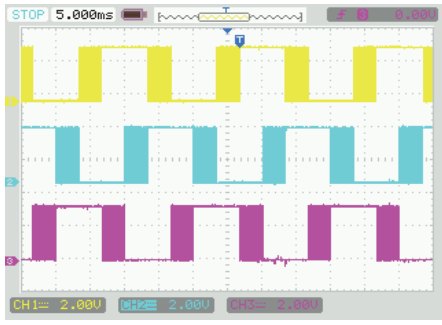
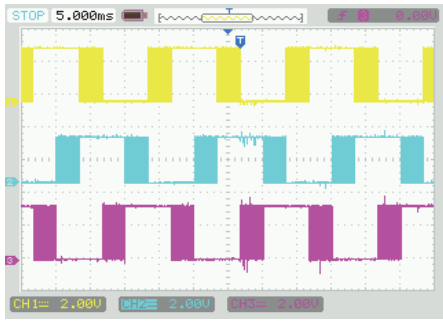


Figure 9: Full system designed setup of three-phase inverter under (120BCM).



(a)



(b)

Figure 10: Upper and Lower PWM of three-phase inverter under 120-BCM.

modulation technique, however, the DC bus voltage is not constant, as shown in Figure 9, and there the instant value it is used in (13).

The switching losses are calculated for two different switches: IRG4PH40UD and C3M0065090D, where the first is an IGBT and the second is a SiC type. The energy at turn-on and turn-off is shown in Table 4. The original values of the currents and voltages at which the energies are obtained are also listed in the same table.

The results of the per cycle calculations for the two types of transistors are listed in Table 5. As expected, the central PWM results in significant switching losses per switch, as well as total losses when IGBT are used. By the improved switching performance of the SiC transistors, the losses are

Table 4: Switches data used for the cycle-by-cycle switching loss calculation.

IRG4PH40UDPbF – IGBT		
Parameter	**Value**	**Conditions**
E_{tot}	7.04 mJ	@ TJ =150°C, I_D=21 A, VCC=800V tail and diode Qrr included
E_{on}	3.39 mJ	
E_{off}	3.64 mJ	
C3M0065090D		
E_{tot}	0.316 mJ	@ TJ =150°C, ID=20 A, VCC=400V
E_{tot}	0.225 mJ	
E_{tot}	0.091 mJ	

further decreased. When the 60° bus clamped modulation is used, the switching losses are reduced almost by half, which is valid for both types of transistors. This is due to the fact that the transistor clamps the DC bus voltage at high phase currents, and switching loses are no longer present. When the 120° bus clamped method is used, the switching losses in both IGBT and SiC switches are decreased more than eight times, compared to the central PWM. The reason for this significant improvement in losses is as follows. Firstly, the 120BCM operates at a lower DC bus voltage compared to the other two modulation techniques. Secondly, the switches are clamped for a much longer period, which avoids commutating high currents. The third and final reason is that only one leg performs the modulation of all phase currents for a period of 60° at lower current values.

The obtained results may differ for different brands and types of switches. If a less expensive design is required, IGBT can be used while still delivering good performance. If SiC devices are used, switching losses are almost entirely eliminated and the heat sink will be much smaller. This is also the case for the DC link capacitor; therefore, the total converter benefits from the specific control strategy.

5. Experimental Setup and Results

Figure 9 presents the full system design of three-phase inverter; the main components of the system are power semiconductor switching, a gate driver circuit that is described in [23, 24], a three-phase filter, a DC power supply, three-phase voltage measurement [10], current measuring circuits, and finally the dsPIC33FG256GB710A as microcontroller. A 900V SiC MOSFET type C3M0065090D from CREE is chosen for the power switch with gate driver circuit [23, 25].

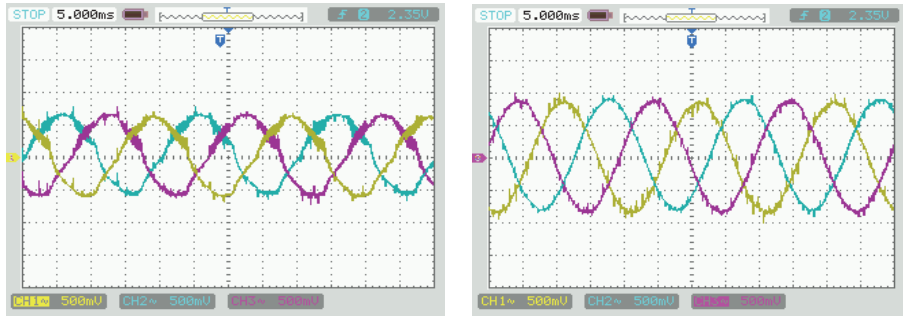
The dsPIC33FG256GB710A microcontroller with Explore 16 Kit that is presented in Figure 9 is used to generate the pulse width modulation and control the three-phase inverter under 120 BCM. The dsPIC is programmed by C language and MPLAB X IDEV3.15 software compiler for programing and debugging [26–28]. This controller is used due to low power consumption and having 9 pins for comparing PWM and 16 pins for 10-Bit A/D converter. The dsPIC is often used in variety of industrial electronic applications.

Figure 10 shows the upper and lower PWM waveforms under 120 BCM generated by dsPIC microcontroller (for

Table 5: Calculation results of the switching losses when different modulation techniques are used.

Modulation type	Central PWM	60° PWM	120BCM
RG4PH40UDPbF-IGBT			
Turn-on losses [W]	25.83	12.96	2.88
Turn-off losses [W]	33.01	17.05	3.96
Total losses [W]	58.84	30.01	6.84
Total inverter losses∗ [W]	353.07	180.06	41.04
C3M0065090D-SiC			
Turn-on losses [W]	3.59	1.80	0.40
Turn-off losses [W]	1.73	0.89	0.21
Total losses [W]	5.32	2.69	0.61
Total inverter losses ∗[W]	31.92	16.14	3.66

∗ **Sum of all switching losses by all six switches**.



(a) Injected phase currents by 120BCM (~200mV/A) CH1 – I_c, CH2 I_a, and CH3 - I_b

(b) Measured phase voltages at the inverter terminals (200V/div) CH1- V_b, CH2- V_c, and CH3 V_a

Figure 11: Three-phase inverter output current and grid voltage.

all test waveforms, PhA-Yelow, PhB-Cyan, and PhC-Pink). The results of the signal detection that performs the partial modulation are depicted in Figure 10. As can be seen, every 60 degrees only one phase is under the PWM and the others are ON/OFF, respectively (upper and lower transistors are opposite under for each phase and PWM).

According to the system setup depicted in Figure 9, the expectable measurement results of three-phase inverter output currents and three-phase grid voltages are shown in the Figure 11. The measurements are taken from the current sensors of the inverter. In this particular application three Hall sensors type CASR 15 NP are used in two-turn configuration which results in an approximate sensitivity of 200 mV/A. The gain of the voltage probe used in this inverter is 1/200 which is enough to attenuate the phase voltages to the acceptable levels of the ADC of the microcontroller.

6. Conclusions

The performance of the proposed 120BCM was extensively verified by means of simulations. The simulation results showed that the 120BCM approach significantly reduces switching losses, compared to state-of-the-art PWM techniques. The advantage in switching losses is in the order of eight times compared to the centered PWM, and roughly four times compared to the 60° bus clamped PWM, for switching losses proportional to current and frequency.

Moreover, the 120BCM is suitable for all types of transistor technologies: MOSFET, IGBT, SiC, and GaN. However, the loss amount will differ depending on the individual switch characteristics; in general, however, switching losses will be significantly reduced. It was also demonstrated by means of simulation that despite the partial modulation of 60 electrical degrees, the quality of the injected phase currents using independent controllers remains significantly below the acceptable level of 5%. Furthermore, the combination of a small nonelectrolytic capacitor, which ensures a long lifetime for the inverter, and improvements in efficiency makes the proposed bus clamped PWM control strategy extremely suitable for renewable energy applications.

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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